REMARKS

This amendment responds to the office action mailed March 9, 2005. In the office action the Examiner:

- rejected claims 2-8 and 25; and
- objected to claims 9-24

After entry of this amendment, the pending claims are: claims 2-25.

Overview of Changes to Claims

Claim 2 has been amended to correct a typographical error and to clarify that the read operation is to the memory device. Support is found in the previously filed claim 2 and in the specification in paragraphs 35 and 44. Therefore, no new matter is introduced by this amendment.

35 USC 103(a) Rejections

Claims 2-4, 6 and 25 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Butler et al. (US 6,720,968) and Harriman (US 6,330,645). Dependent claims 7 and 8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Butler et al. (US 6,720,968) and Harriman (US 6,330,645) and Lo et al (US 6,115,760). Claim 5 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Butler et al. (US 6,720,968) and Harriman (US 6,330,645) and Takada et al. (US 6,633,961). The Applicants disagree and traverse.

Harriman discloses a memory system to address coherency issues for multiple memory access streams issued by multiple memory controller access devices (abstract, lines 1-2). Coherency of memory with multiple controllers involves a system in which the same data is written to at least a portion of the address space of some or all of the memory controllers [emphasis added] (col. 2, lines 49-67). Thus, a coherency issue arises if commands are sent to at least two different memory devices storing the same data at the same addresses. In contrast, the claims in the present application address a controller trying to read data from the same address previously written to the same memory device. If these operations are performed in Harriman, the corresponding data is simply read, i.e., a coherency issue does not arise. Therefore, Harriman addresses a different problem than that disclosed in the present application.

As noted by the Examiner in the present Office Action (p. 4, lines 3-5 of March 28, 2005 office action), Butler does not suggest or teach that the controller performs a predefined operation on a read command when a second address corresponding to the read command is the same as the first address. Since Butler concerns a video capture system with a virtual dual ported memory (to enable both video device and CPU access), but no need for cache coherence or memory coherence mechanisms, there would appear to be no motivation to combine Butler et al. with Harriman. Harriman concerns a system having multiple memory controllers and multiple CPUs with memory coherence and complexity issues completely lacking in the Butler et al. system. Thus, the combination of Butler et al. and Harriman is not *Prima Facie* obvious. Claims 2 and its dependent claims, and claim 25 are novel and unobvious over the prior art of record. Removal of this ground for rejection is requested.

Prior Art Made of Record

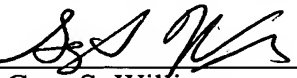
The Examiner indicated that prior art made of record and not relied upon is considered pertinent to the Applicant's disclosure. Under 37 CFR 1.111(b), "(t)he reply must present arguments pointing out the specific distinctions believed to render the claims, including any newly presented claims, patentable over any applied references" (emphasis added). It is respectfully noted that the Office Action did not apply any such prior art made of record to any of the pending claims.

CONCLUSION

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: May 27, 2005



31,066 (Reg. No.)

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